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Paper Code : BCAC202 Computer Architecture

UPID : 200052

Time Allotted : 3 Hours *Full Marks :70*

The Figures in the margin indicate full marks.

Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer *any ten* of the following : [1 x 10 = 10]

(I) The IR stores which one of the following?

1. An instruction that has been decoded.
2. An instruction that have been fetched from memory.
3. An instruction that has been executed.
4. The address of the next instruction to be executed.

(II) Which of the following set of gates can be used to realize a full-adder?

1. Two half-adders and one OR gate
2. Two OR gates and one half-adder
3. One half-adder and two OR gates
4. One OR gate and one half-adder

(III) What is micro code?

(IV) Causing the CPU to step through a series of micro operations is called _____

(V) Convert binary number $(10010110)_2$ into octal number

(VI) A processor performing fetching and decoding of different instruction during the execution of another instruction is

1. Cache.
2. Parallel Processing.
3. Pipelining.
4. All of the Above.

(VII) How many types of modes of I/O Data Transfer?

1. 2
2. 3
3. 4
4. 5

(VIII) In memory-mapped I/O _____

1. The I/O devices have a separate address space
2. The I/O devices and the memory share the same address space
3. A part of the memory is specifically set aside for the I/O operation
4. The memory and I/O devices have an associated address space

(IX) 10's complement of decimal 2389 is _____

(X) Which of the following is true about Normalization?

1. Floating point numbers are usually normalized
2. Exponent is adjusted so that leading bit (MSB) of mantissa is 1
3. Since it is always 1 there is no need to store it
4. All of the above

(XI) ——- is contained by the page table.

A. page size B. base address of every page C. page offset D. Page

(XII) An instruction cycle refers to which one of the following?

1. Fetching an instruction
2. Executing an instruction
3. Fetching an instruction, decoding it, reading the contents of the effective address of the operands and executing the instruction

Group-B (Short Answer Type Question)

Answer *any three* of the following : [5 x 3 = 15]

2. Explain different type of Interrupts. [5]
3. Explain the Memory Hierarchy of a Computer System with diagram. [5]
4. What are the hazards of instruction pipeline? [5]
5. Explain the difference between hardwire control and microprogrammed control? [5]
6. The 8-bit registers AR, BR, CR, and DR initially have the following values: AR= 11010010, BR= 11100011, CR= 10111001 , DR= 10101011. Determine the 8-bit values in each register after the execution of the following sequence of micro operations. [5]
   AR <-AR + BR
   CR <- CR ^ DR, BR <- CR + 1
   AR <-AR – CR

Group-C (Long Answer Type Question)

Answer *any three* of the following : [15 x 3 = 45]

7. A. Draw the circuit diagram of the 4 bit binary adder-Subtractor and explain it? [15]
   B. Draw the circuit diagram of 4-bit arithmetic circuit and explain with the function table?
   C. Explain the bus system for four register with diagram?
8. A. What is parallel processing? [15]
   B. What is arithmetic pipelining?
   C. Describe the working principle of pipeline?
   D. What is Structural Hazard explain with an example?
   E. What is vector processing?
9. A. What is RISC? [15]
   B. Write some advantages of RISC?
   C. Explain the concept of sequential processing pipelining and parallel processing with example?
   D. What is the benefit of pipelining?
10. A. Explain DMA with block diagram. [15]
    B. Describe input-output processor (IOP) with block diagram.
11. A. Differentiate between Logical and Arithmetic shift with example. [15]
    B. Explain about different addressing modes.
    C. Convert $(4768)_{10}$ to hexadecimal format.

*** END OF PAPER ***